ELIZADE UNIVERSITY, ILARA-MOKIN,

ONDO STATE

FACULTY OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

SECOND SEMESTER EXAMINATION, 2018/2019 ACADEMIC SESSION

COURSE TITLE: ELECTRONIC CIRCUITS II

COURSE CODE: EEE 322

EXAMINATION DATE: 10th July, 2019

COURSE LECTURER: Dr. Akinwumi A. Amusan

TIME ALLOWED: 3 hours

HOD's SIGNATURE

INSTRUCTIONS:

1. ANSWER ANY FIVE QUESTIONS
2. ANY INCIDENT OF MISCONDUCT, CHEATING, POSSESSION OF UNAUTHORIZED MATERIALS DURING EXAM SHALL BE SEVERELY PUNISHED.
3. YOU ARE NOT ALLOWED TO BORROW CALCULATORS AND ANY OTHER WRITING MATERIALS DURING THE EXAMINATION.
4. ELECTRONIC DEVICES CAPABLE OF STORING AND RETRIEVING INFORMATION ARE PROHIBITED.
5. DO NOT TURN TO YOUR EXAMINATION QUESTION PAPER UNTIL YOU ARE TOLD TO DO SO.

Question #1 (12 Marks)

(a) The circuit in Figure Q1a shows a diagram for an automobile alarm circuit used to detect certain undesirable conditions. The three switches are used to indicate the status of the door by the driver's seat, the ignition, and the headlights, respectively.

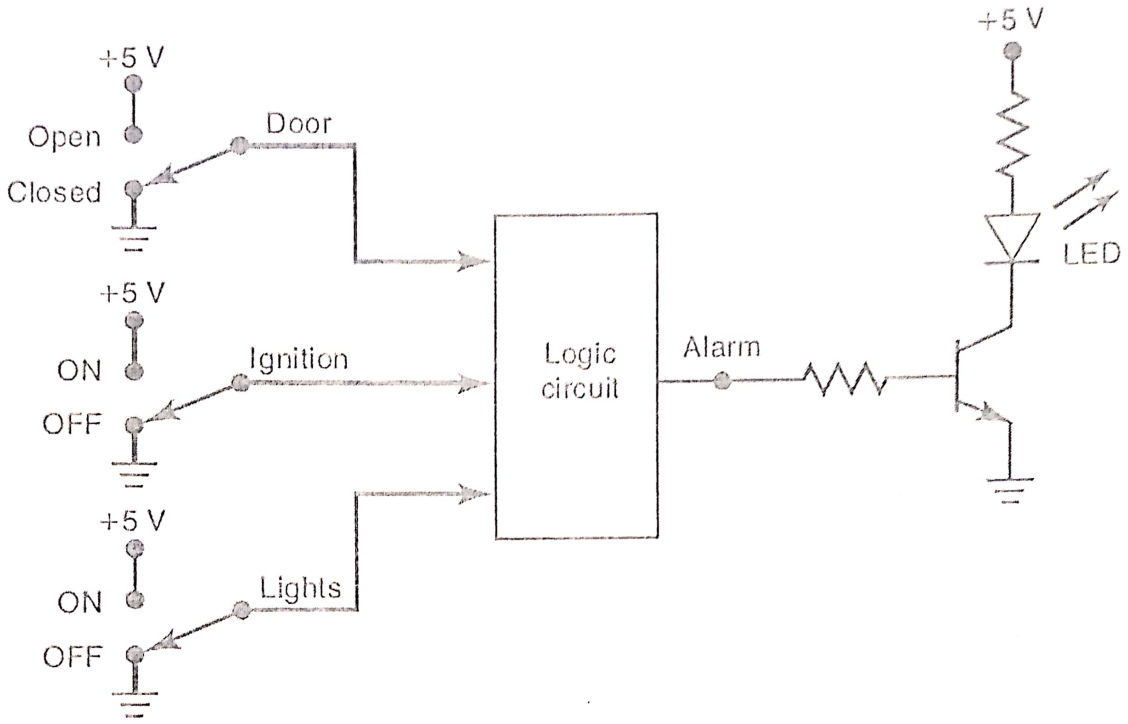

Figure Q1a

Design the logic circuit with these three switches as inputs so that the alarm will be activated whenever either of the following conditions exists:

- The headlights are on while the ignition is off.
- The door is open while the ignition is on. (6)

(b) Define the following terms as it applies to non – ideal pulse

(i) Ringing (1)

(ii) Overshoot (1)

(iii) Rise time (1)

(c) The waveform in Figure Q1b shows input and output timing diagram in a logic circuit

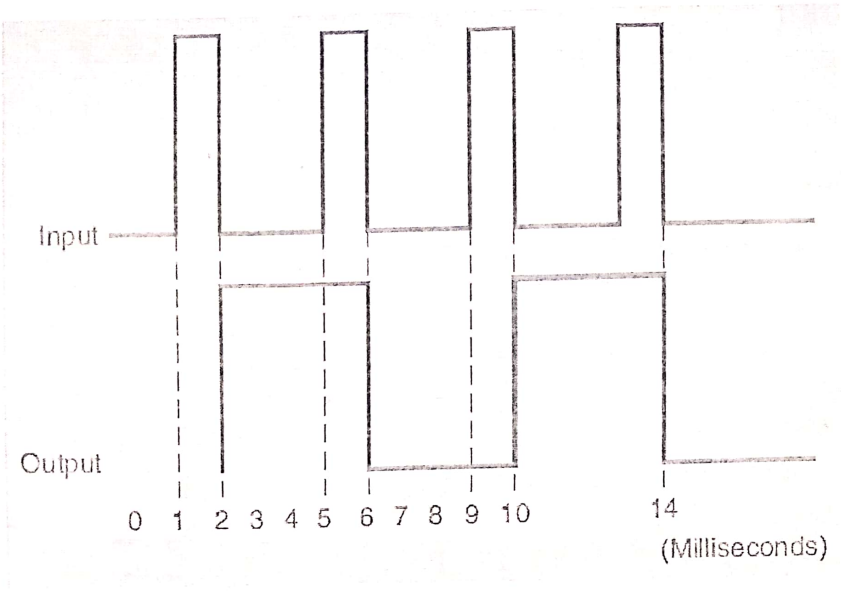

Figure Q1b

(i) Determine the active-HIGH duty cycle of the input waveform? (1)

(ii) What is the frequency of the input waveform in Hz? (1)

(iii) What is the frequency of the output waveform in Hz? (1)

Question #2 [12 Marks]

(a) A BCD code is being transmitted to a remote receiver. The bits are A_3, A_2, A_1, and A_0, with A_3 as the MSB. The receiver circuitry includes a BCD validity checker circuit that examines the received code to see if it is a legal BCD code (i.e., ≤ 1001). Design this circuit to produce a HIGH only if a valid BCD number is received. Use K-map for simplification. (6)

(b) Add the following BCD numbers:

(i) 1001000001001001 + 0000100100100101 (2)

(ii) 010001011000 + 010000010111 (2)

(c) The following signed binary numbers given are expressed in 2's complement notation, Evaluate:

11100111 + 00010000 -- 00010011 + 11101000 (2)

Question #3 (12 Marks)

(a) Given the logic circuit in Figure Q3

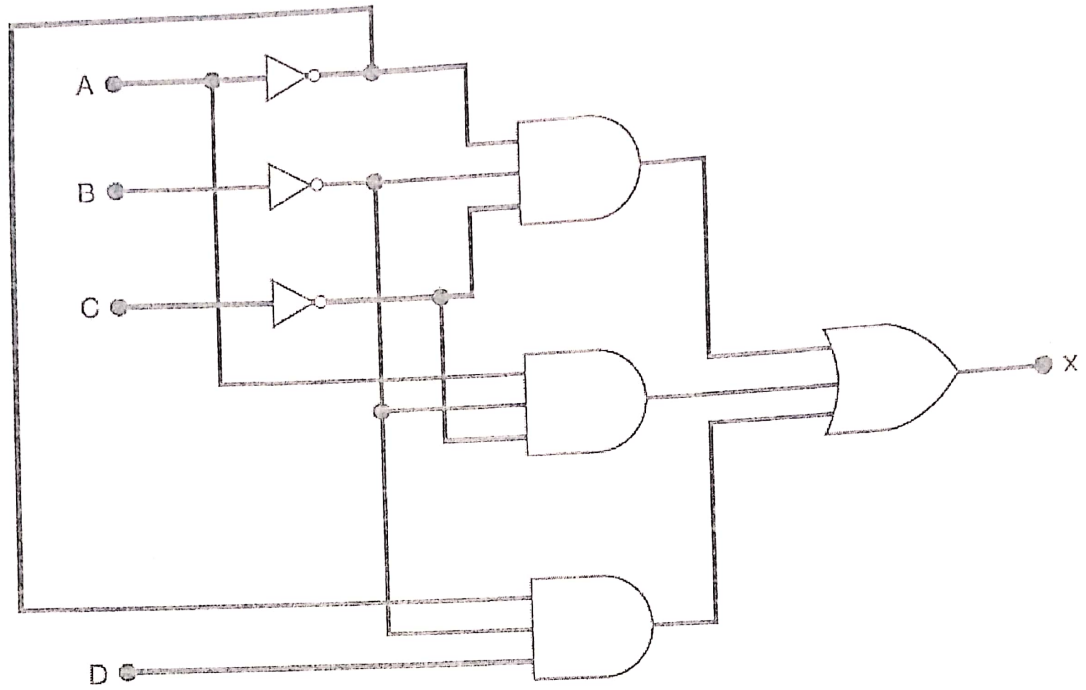

Figure Q3

(i) Write the Boolean expression for output x (2)

(ii) Determine the value of x for all possible input conditions using a truth table. (3)

(iii) Simplify the truth table using K-map or otherwise (2)

(iv) Draw the simplified logic circuit (1)

(b) Determine the binary and decimal value of the floating-point number
0 10011000 10000100010100110000000 (3)

(c) Convert the hexadecimal number $AE8F_{16}$ to binary (1)

Question #4 (12 Marks)

(a) The circuit in Figure Q4a shows four switches that are part of the control circuitry in a copy machine. The switches are at various points along the path of the copy paper as the paper passes through the machine. Each switch is normally open, and as the paper passes over a switch, the switch closes. It is impossible for switches SW1 and SW4 to be closed at the same time.
Design the logic circuit to produce a HIGH output whenever two or more switches are closed at the same time. Use K-mapping and take advantage of the don't-care conditions. (8)

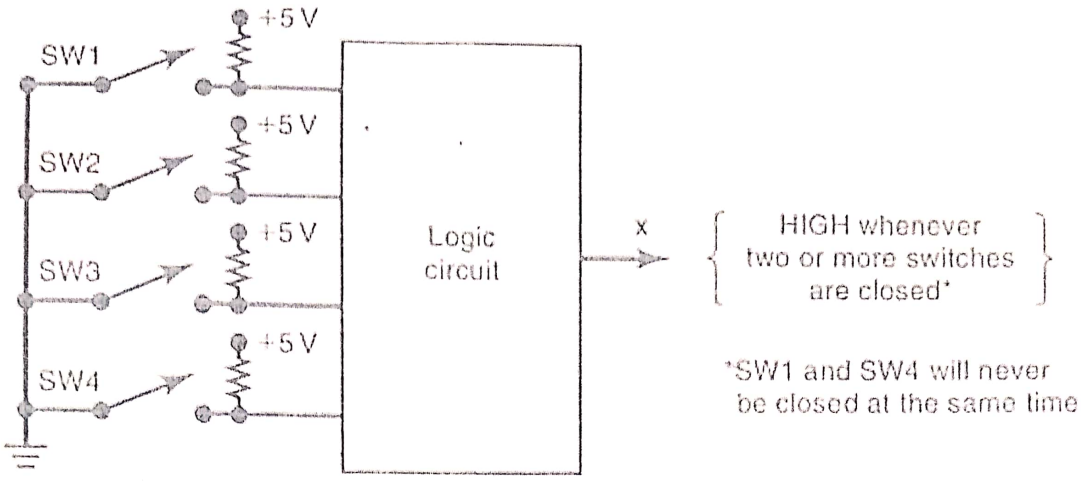

Figure Q4a

(b) The timing diagram for the clock signal and digital input is shown in Figure Q4b

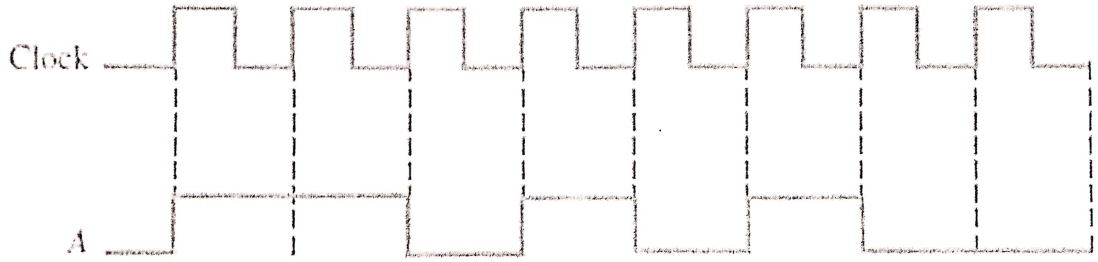

Figure Q4b

(i) What is the total serial transfer time for the eight bits if the clock frequency is 10 MHz? (1)

(ii) What is the total time to transfer the same eight bits in parallel? (1)

(c) List the various categories of PLDs (2)

Question #5 [12 Marks]

(a) A jet aircraft employs a system for monitoring the rpm, pressure, and temperature values of its engines using sensors that operate as follows:

RPM sensor output = 0 only when speed < 4800 rpm
P sensor output = 0 only when pressure < 220 psi
T sensor output = 0 only when temperature < 200 °F

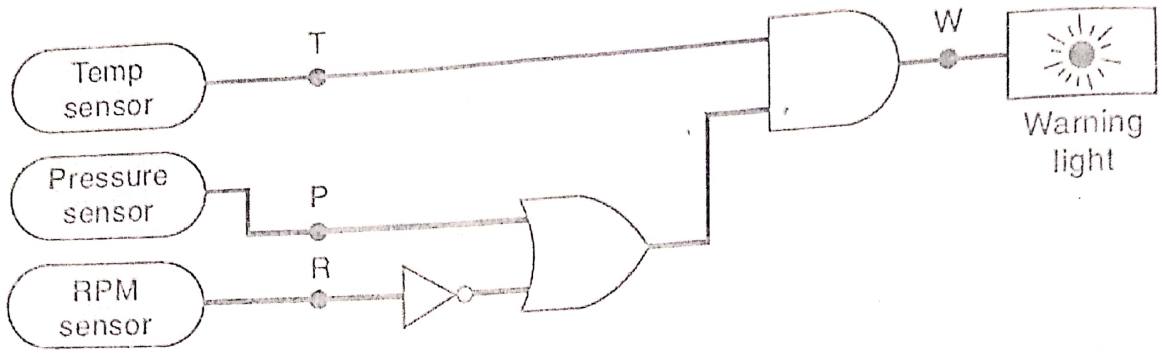

Figure Q5a

Figure Q5a shows the logic circuit that controls a cockpit warning light for certain combinations of engine conditions. Assume that a HIGH at output *W* activates the warning light. Determine what engine conditions will give a warning to the pilot? (3)

(b) Simplify the logic circuit in Figure Q5b using Boolean algebra.

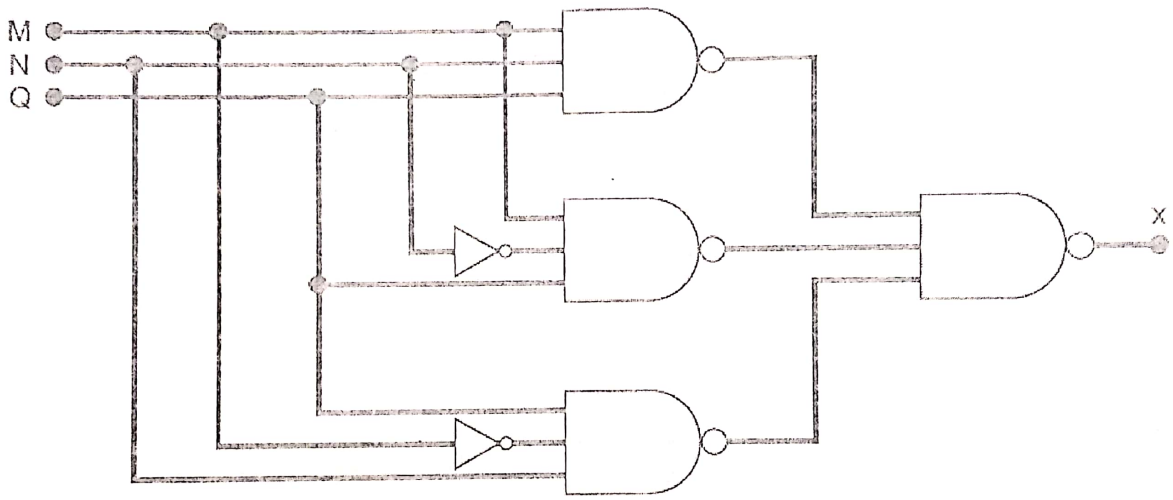

Figure Q5b

(4)

(c) Construct the corresponding logic circuit using AND, OR gates and INVERTERs

$$x = \overline{(\overline{AB} + CD)}$$ (2)

(d) Use K-map to simplify the Boolean expression $y = \overline{C}\,(\overline{A}\,\overline{B}\,D + \overline{D}) + \overline{A}\,\overline{B}\,C + \overline{D}$

(3)

Question #6 (12 Marks)

(a) Differentiate between synchronous and asynchronous counters (2)

(b) A 3-bit asynchronous binary counter is shown in Figure Q6b. Each D flip-flop is positive edge-triggered and has a propagation delay for 10 nanoseconds (ns).

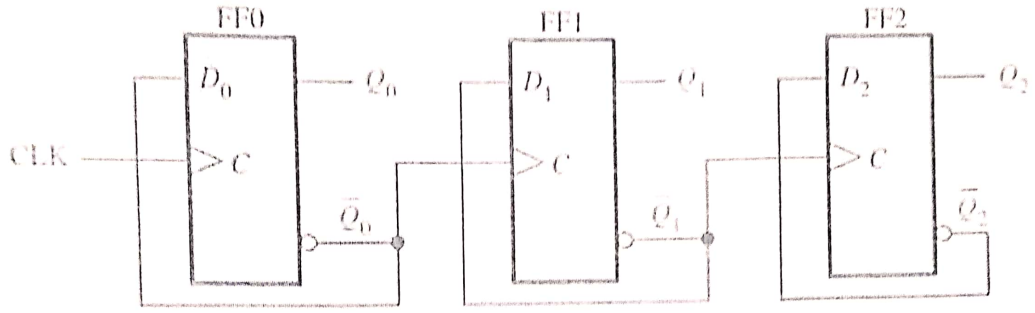

Figure Q6b

(i) Develop a timing diagram showing the Q output of each flip-flop, and determine the total propagation delay time from the triggering edge of a clock pulse until a corresponding change can occur in the state of Q2. (4)

(ii) Determine the maximum clock frequency at which the counter can be operated. (1)

(iii) How many D flip-flops are required for a divide-by- 64 frequency division circuit? (1)

(c)

(i) Draw the schematic diagram for the NOR and NAND gate latch (2)

(ii) Write the truth table for an active-high input S-R latch (2)

Question #7 (12 Marks)

(a) A certain housing complex comprises four building towers, namely A, B, C, and D. Each of the four towers has a separate point for the power supply, which is connected to the electrical meter boxes of individual flats. Each power supply point has a voltage detecting sensor that outputs a HIGH if the supplied power meets the minimum voltage requirement criteria. The housing complex has an alternative power supply source that is switched on in case emergency power is required. An emergency is identified when at least two of the four towers have a voltage less than the minimum; that is, when at least two sensors output is LOW.
Design a logic circuit to trigger the emergency power supply. It should accept the outputs of the four sensors A, B, C, and D as inputs and output a HIGH when at least two of them are LOW. (7)

(b) Define the following terms with respect to operating characteristics of logic families

(i) Propagation delay (1)

(ii) Fan out (1)

(iii) Noise immunity (1)

(c) The input/output voltage specifications for the standard TTL family are listed in Table Q7c.

Table Q7c

Parameter	Min (V)	Typical (V)	Max (V)
V_{OH}	2.4	3.4	
V_{OL}		0.2	0.4
V_{IH}	2.0		
V_{IL}			0.8

Use these values to determine the following.

(i) The maximum-amplitude noise spike that can be tolerated when a HIGH output is driving an input. (1)

(ii) The maximum-amplitude noise spike that can be tolerated when a LOW output is driving an input. (1)